AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1-13. (Canceled)

14. (Currently Amended) A filtering method comprising:

receiving first and second differential inputs, said differential inputs each comprising a first signal and a second signal, the second input having been received prior to the first input;

biasing [[the]]first and second differential input pairs with the first and second differential inputs, respectively;

weighting the first and second differential inputs by modulating [[the]]a gain of at least one of the differential input pairs; and

tapping [[the]]first and second output nodes to obtain a filtered signal, wherein the first and second output nodes are connected to [[the]]transistors of the differential input pairs which are biased by the ~~inverted inputs~~first signals and the ~~non-inverted inputs~~second signals, respectively.

15. (Original) The method of claim 14, wherein the output nodes are coupled to at least one load selected from the group consisting of a regenerative latch, a passive load, an active filter, and an amplifier.

16. (Currently Amended) The method of claim 14, wherein the gain is modulated by altering ~~the~~ tail currents of the differential input pairs.

17. (Currently Amended) The method of claim 14, wherein the gain is modulated by altering ~~the~~ tail currents provided by a plurality of variably controlled current sources.

18. (Currently Amended) The method of claim 14, wherein the gain is modulated by altering ~~the~~ one or more channel widths ~~of the channels of~~ in the transistors.

19. (Currently Amended) The method of claim 14, further comprising inducing an offset by connecting first and second offset-inducing differential input pairs in parallel to the first and second differential input pairs, wherein ~~the~~ transistor channel widths in at least one ~~transistor~~ differential input pair are mismatched.

20. (Currently Amended) The method of claim 19, further comprising inducing an offset in a third differential input, the third differential input having been received after the first [[signal]]differential input.

21. (Currently Amended) The method of claim 19, further comprising equally and oppositely offsetting ~~the~~ tail currents of the first and second offset-inducing differential input pairs from a nominal current level relative to ~~the~~ tail currents for the first or second differential input pairs, respectively.

22. (Currently Amended) The method ~~circuit~~ of claim 14, wherein the filtered signal is also amplified and offset.

23. (Currently Amended) The method of claim 14, wherein the transistors of the differential input pairs are [[n]]p-channel MOSFET transistors.

24. (Currently Amended) The method of claim 14, further comprising receiving a third differential ~~signal~~input, the third ~~signal~~differential input having been received after the first [[signal]]differential input, biasing a third differential input pair with the third ~~signal~~differential input, and weighting the third ~~signal~~differential input by modulating the gain of at least one of the differential input pairs.

25. (Currently Amended) A communications system comprising:

(a) a transmitter producing a differential voltage signal comprising a first voltage and a second voltage;

(b) a receiver comprising:

(1) a sample-and-hold circuit that receives the differential voltage signal and samples and holds values of the differential voltage signal; and

(2) a filter circuit comprising:

a first differential transistor pair biased by a first differential input received from the sample-and-hold circuit;

a second differential transistor pair biased by a second differential input, the second differential input having been received from the sample-and-hold circuit prior to the first differential input;

at least one current source coupled to provide tail currents for the differential transistor pairs;

wherein the transistors which are biased by present and previous ~~inverted inputs~~first voltages have a first output terminal; and

wherein the transistors which are biased by present and previous ~~non-inverted inputs~~second voltages have a second output terminal.

26. (Original) The communications system of claim 25, wherein the transmitter and the receiver reside on different circuit boards.

27. (Original) The communications system of claim 25, wherein the transmitter and the receiver reside on different integrated circuit die.

28. (Currently Amended) The communications system of claim 25, wherein the filter circuit further comprises first and second offset-inducing differential transistor pairs connected in

parallel to the first and second differential transistor pairs, respectively, wherein [[the]] one or more channel widths [[of]] in the transistors in each differential transistor pair are not equal and wherein the difference in channel width in the offset-inducing differential transistor pairs is opposite that of the first and second differential transistor pairs.

29. (New) A filter circuit comprising:

a first differential transistor pair biased by a first differential input comprising a present first voltage signal and a present second voltage signal;

a second differential transistor pair biased by a second differential input comprising a previous first voltage signal and a previous second voltage signal, the second differential input having been received prior to the first differential input; and

at least one current source coupled to provide tail currents for the differential transistor pairs, said tail current of the first differential transistor pair being different from said tail current of the second differential transistor pair,

wherein the transistors which are biased by present and previous first voltage signals have a first output node, the transistors which are biased by present and previous second voltage signals have a second output node, and the tail current differential is provided by a difference in channel widths between the first and second differential transistor pairs.

30. (New) The filter circuit of claim 29, wherein the output nodes are coupled to at least one load selected from the group consisting of a regenerative latch, a passive load, an active filter, and an amplifier.

31. (New) The filter circuit of claim 29, wherein the tail currents are provided by a plurality of variably controlled current sources.

32. (New) The filter circuit of claim 29, wherein the output nodes provide an amplified, offset and filtered differential signal.

33. (New) A filter circuit comprising:

a first differential transistor pair biased by a first differential input comprising a present first voltage signal and a present second voltage signal;

a second differential transistor pair biased by a second differential input comprising a previous first voltage signal and a previous second voltage signal, the second differential input having been received prior to the first differential input;

at least one current source coupled to provide tail currents for the differential transistor pairs; and

first and second offset-inducing differential pairs connected in parallel to the first and second differential transistor pairs, respectively,

wherein the transistors which are biased by present and previous first voltage signals have a first output node, and the transistors which are biased by present and previous second voltage signals have a second output node.

34. (New) The filter circuit of claim 33, wherein channel widths of the transistors in each differential transistor pair are not equal and wherein the difference in channel width in the offset-inducing differential pairs is opposite that of the first and second differential transistor pairs.

35. (New) The filter circuit of claim 34, wherein the tail currents for the first and second offset-inducing differential pairs are equally and oppositely offset from a nominal current level relative to the tail current for the first or second differential transistor pairs, respectively.

36. (New) The filter circuit of claim 35, wherein the output nodes provide an amplified, offset and filtered differential signal.

37. (New) The filter circuit of claim 33, wherein the output nodes provide an amplified, offset and filtered differential signal.

38. (New) A filter circuit comprising:

a first differential transistor pair biased by a first differential input comprising a present first voltage signal and a present second voltage signal;

a second differential transistor pair biased by a second differential input comprising a previous first voltage signal and a previous second voltage signal, the second differential input having been received prior to the first differential input; and

at least one current source coupled to provide tail currents for the differential transistor pairs,

wherein the transistors which are biased by present and previous first voltage signals have a first output node, the transistors which are biased by present and previous second voltage signals have a second output node, the transistors of the differential transistor pairs are p-channel MOSFET transistors, and a filtered output signal is provided at the output nodes.

39. (New) The filter circuit of claim 38, wherein the output nodes provide an amplified, offset and filtered differential signal.

40. (New) A filter circuit comprising:

a first differential transistor pair biased by a first differential input comprising a present first voltage signal and a present second voltage signal;

a second differential transistor pair biased by a second differential input comprising a previous first voltage signal and a previous second voltage signal, the second differential input having been received prior to the first differential input;

a third differential transistor pair being biased by a third differential input comprising a subsequent first voltage signal and a subsequent second voltage signal, the third differential input being received after the first differential input; and

at least one current source coupled to provide tail currents for the differential transistor pairs,

wherein the transistors which are biased by present and previous and subsequent first voltage signals have a first output node, and the transistors which are biased by present and previous and subsequent second voltage signals have a second output node.

41. (New) The filter circuit of claim 40, wherein the output nodes provide an amplified, offset and filtered differential signal.

42. (New) A filter circuit comprising:

a first differential transistor pair biased by a first differential input comprising a present first voltage signal and a present second voltage signal; and

a second differential transistor pair biased by a second differential input comprising a previous first voltage signal and a previous second voltage signal, the second differential input being received prior to the first differential input,

wherein the transistors which are biased by present and previous first voltage signals have a first output node, and the transistors which are biased by present and previous second voltage signals have a second output node.